7B80 and 7B85

7B85 Features:

Δ Time Measurements with CRT Readout

Delayed Time Measurements with CRT Readout

Vertical Trace Separation Between Two Delayed Sweeps

Both Feature:

1 ns/div to 5 s/div Calibrated Time Bases

Triggering to 400 MHz

Variable Trigger Holdoff

Peak-to-Peak Auto Triggering

The 7B80 and 7B85 are horizontal time bases recommended for use with 7700, 7800 and 7900 Series Mainframes to provide optimum bandwidth/sweep-speed compatibility. (Each may be used in any slower 7000 Series Mainframe with some reduction in sweep accuracy at the fastest sweep speed.)

Either plug-in can be used separately as an independent single time base, or they can be combined in any mainframe with two horizontal compartments for delaying and delayed operation.

X-Y displays are available using a 7B80 with Option 02. A front-panel button (DISPLAY MODE) selects either normal sweep or X-Y display. Both signals are applied to vertical (Y) amplifiers, and the desired horizontal (X) signal is then routed through plug-in and mainframe trigger paths to the 7B80. An X-Y mode selection then applies the signal to the horizontal deflection system.

CHARACTERISTICS

Characteristics are common to both units unless otherwise noted.

Sweep Rates — 5 s/div to 10 ns/div in 27 steps (1-2-5 sequence). X10 MAGNIFIER extends fastest calibrated sweep rate to 1 ns div. The uncalibrated VARIABLE is continuous to at least 2.5 times the calibrated sweep rate.

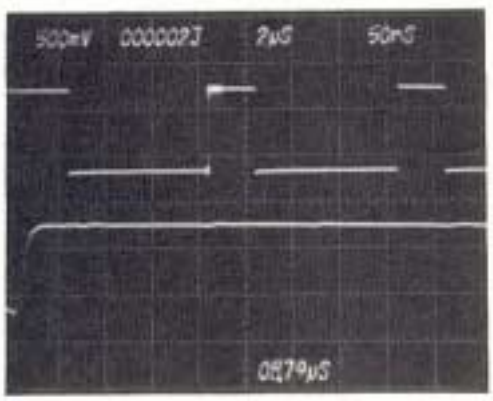


figure 1. Delaying and delayed sweeps are shown with the mainframe selecting ALT sweep modes. The delay time to the start of the delayed sweep is digitally presented on the lower edge of the CRT.

7B80

Delayed Time Base

Sweep Accuracy — Measured over the center 8 div, +15°C to +35°C, in the 7700, 7800, or 7900 Series Mainframe. Derate accuracies by an additional 1% for 0°C to +50°C.

Time/Div[1]	Unmagnified	Magnified
5 s/div to 1 s/div	4%	Unspecified
0.5 s/div to 50 ns/div	1.5%	2.5%
20 ns/div to 10 ns/div	2.5%	4.0%

[1]Fastest calibrated sweep rate is limited by 7700 and 7500.

Trigger Holdoff Time —

Minimum Holdoff Setting	5 s/div to 1 μs/div	2 times TIME/DIV setting or less
	0.5 μs/div to 10 ns/div	2.0 μs or less
Variable Holdoff Range	Extends holdoff time through at least 2 sweep lengths for rates of 20 ms/div or faster	

Δ Time Range — 0 to at least 9 times TIME/DIV setting.

Δ Time Accuracy — (+15°C to +35°C)
Within (0.5% measurement + 0.3% of TIME/DIV setting + 1 least significant digit) from 20 ms/div to 100 ns/div.

Trace Separation Range — Functional only in Δ Delay Time mode when alternating or chopping between time-base units. The second delayed sweep display can be vertically positioned at least 3 div below the first delayed sweep display.

Delay Time Range — 0.2 or less to at least 9.0 times TIME/DIV setting.

Jitter — 0.02% of TIME/DIV setting + 0.1 ns, or less.

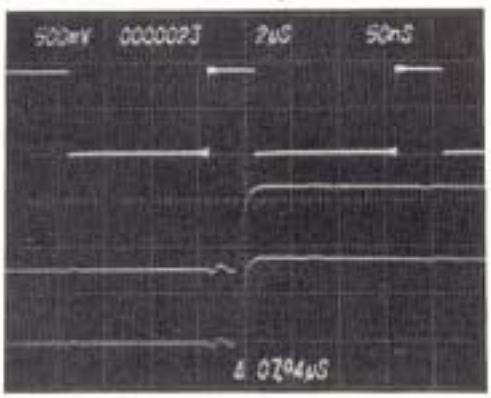
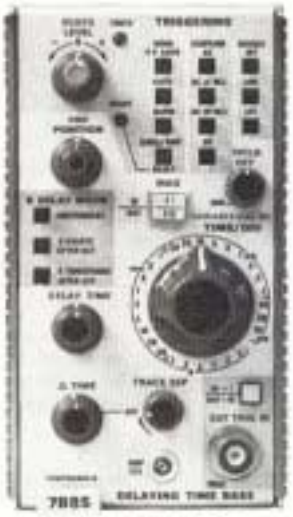


figure 2. With the mainframe still selecting ALT sweeps, delaying and both delayed sweeps are shown. The digital readout on the lower CRT edge shows the time between the two sweep delays. The TRACE SEPARATION knob is used to position the second delayed sweep below the first delayed sweep with up to 3 div of separation.

7B85



Δ Delaying Time Base

TRIGGERING

Triggering Sensitivity (Auto and Norm Modes) — (from repetitive signals)

Coupling	Triggering Frequency Range[1]	Min Signal Required Int	Min Signal Required Ext
Ac	30 Hz to 50 MHz	0.3 div	50 mV
	50 MHz to 400 MHz	1.5 div	250 mV
Ac LF REJ[2]	30 kHz to 50 MHz	0.3 div	50 mV
	50 MHz to 400 MHz	1.5 div	250 mV
Ac HF REJ	30 Hz to 50 kHz	0.3 div	50 mV
Dc[3]	Dc to 50 MHz	0.3 div	50 mV
	50 MHz to 400 MHz	1.5 div	250 mV

[1]Triggering frequency ranges are limited to the frequency of the vertical system when operating in the Internal mode.

[2]Will not trigger on sine waves of less than 8 div Int, or 3 V Ext, at or below 60 Hz.

[3]Triggering Frequency Range for dc coupling applies to frequencies above 30 Hz when operating in the Auto triggering mode.

Single Sweep — Requirements are same as for repetitive inputs.

Internal Trigger Jitter — 0.1 ns or less at 400 MHz.

Sensitivity (P-P AUTO Mode) — (ac or dc coupling)

Triggering Frequency Range	Min Signal Required Int	Min Signal Required Ext
200 Hz to 50 MHz	0.5 div	125 mV
50 MHz to 400 MHz	1.5 div	375 mV
Low Frequency Response: At least 50 Hz	2.0 div	500 mV

External Trigger Input — Max input voltage is 250 V (dc + peak ac). Input R and C is 1 MΩ within 5% and 20 pF within 10%. The level range (excluding P-P AUTO) is at least ±1.5 V in EXT ÷ 1, and at least ±15 V in EXT ÷ 10.

7B80 Option 02 —

X-Y Phase Shift — (Determined by the circuitry in mainframe) — For mainframe without X-Y horizontal compensation, the mainframe phase shift specifications are retained for frequencies of 50 kHz and below. For mainframes with optional X-Y horizontal compensation, the extra delay adds to the phase shift error above 50 kHz.

ORDERING INFORMATION

7B80 Time Base

7B85 Delaying Time Base

7B80 OPTION

Option 02, X-Y